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DESIGN AND IMPLEMENTATION OF MAC UNIT BY USING VEDIC SUTRAS

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Abstract:
In this paper presents the design of a MAC unit that is based on the Vedic multiplier and its application, for the processing of equations that solely contain multiplication terms. The use of Vedic multiplier as a replacement of the Vedic square helps in reduction of area and time delay. In this project, the Vedic multiplier is compared to the Vedic square both are based on the Urdhav Triyabhya sutra and also Vedic multiplier has based on the another two sutras those are Yavadunam and Nikhilam sutras of Vedic mathematics. Duplex property of this sutras forms the basis of Vedic multiplier. Using this, logic gates are eliminated from the initial level of 4*4 bit and 8*8 bit Vedic multiplier architecture. This leads to an increase in speed by means of reduced toggling of gates and time. Moreover, it reduces total area of gates and time delay of MAC unit (with Vedic multiplier and PIPO adder). Relative to the MAC with Vedic Square and Koggestone Adder. MAC unit based on Vedic multiplier PIPO adder is used to run the multiplication process in Urdhav, Nikhilam and Yavadunam of Vedic sutras.

***Key words*: MAC unit, Vedic square, Vedic multiplier**

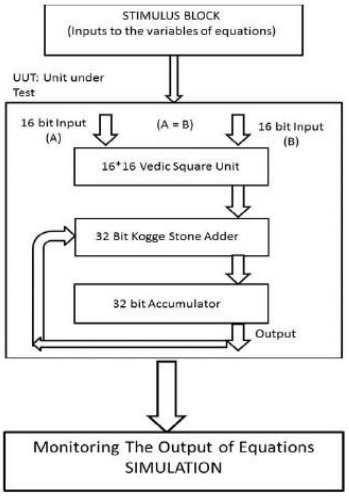


Fig.1: Vedic square with Koggstone Adder.

1. INTRODUCTION

The MAC unit comprises of a Vedic Square, an koggstone adder and an accumulator. The application of MAC unit, include the processing of equations involving square terms only Vedic mathematics is part of four Vedas (books of wisdom). It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus [3]. It is an ancient solution to various mathematical problems. It is based on 16 principles or 'sutras' [4]. This is the existing architecture for faster processing of equations with square terms only, using limited hardware. The existed design (Fig.1) uses one 16x16 Vedic multiplier using „Urdhva Tiryagbhyam" algorithm [6-10], 32 bit accumulator using carry save adder, and one 32 bit register.

The following equations were run using the existed MACunit:*Equation (1): Pythagoras Theorem*

$B^2 + P^2 = H^2$

Here, B= Base of triangle, P= Perpendicular, H= Hypotenuse

Equation (2): Equation of Ellipse

$(x/a)^2 + (y/b)^2 = 1$

Here, (x,y) are coordinates of any point on the ellipse a, b are the radius on the X and Y axis respectively

Equation (3): Equation of Circle with Center (0, 0)

$x^2 + y^2 = r^2$.

Here, x, y are coordinates of any point on the circle r is the radius of the circle. MAC Unit based on the Vedic Square and koggstone adder performance is only reduction of logic gates or area. So, we go for vedic multiplier it has the reduce the area and time delay, as well as high speed. That is MAC Unit based on VedicmultiplierwithPIPOAdder.

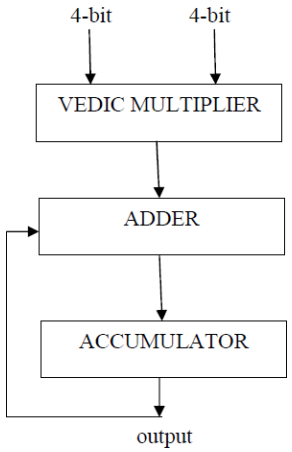


Fig.2. MAC Architecture using Vedic Multiplier and Sparse Accumulator

The general MAC architecture consists of a conventional multiplier, adder and an accumulator. Where the output is added to the previous MAC output result by an accumulate adder. The Multiply-Accumulate (MAC) unit is extensively used in microprocessors and digital signal processors for data-intensive applications, such as filtering, convolution, and inner products. Most digital signal processing methods use nonlinear functions such as discrete cosine transform (DCT) or discrete wavelet transform (DWT) or FFT/IFFT computations that can be efficiently accelerated by dedicated MAC units. Because they are basically accomplished by repetitive application of multiplication and addition, the speed of the multiplication and addition determines the execution speed and performance of the entire computation. As the multiplier exhibits inherently long delay among the basic operational blocks in digital system, the multiplier determines the critical path. In order to improve the speed of the MAC unit, there are two major bottlenecks. The first is the partial products reduction network that is used in the multiplication block and the second is the accumulator. Both of these stages require addition of large operands that involve long paths for carry propagation.

The main key to the proposed architecture is using the Vedic multiplier to design the MAC unit and compare the performance with the conventional MAC units in terms of area, speed and number of resources. It is well known fact that the speed of MAC is governed by the speed of the multiplier. The Vedic multiplier uses “Urdhva Tiryagbhyam” algorithm. The authors in [3] use Vedic multiplier based on the ancient algorithms (sutras) for multiplication. This work is based on the sutra "Nikhilam Sutra" and “Yavadhunam Sutra also. Those are all sutras based on vedic mathematics. This project present a technique to modify the architecture of the Vedic multiplier by using existing methods in order to reduce. The proposed design shows considerable improvements in terms of area and time delay. The major applications of Multiply-accumulate (MAC) unit are microprocessors, logic units and digital signal processors, since it determines the speed of the overall system. The efficient designs by MAC unit are Nonlinear Computation like Discrete Cosine or wavelet Transform (DCT), FFT/IFFT. Since, they are basically executed by insistent application of multiplication and addition, the entire speed and performance can be compute by the speed of the addition and multiplication taking place in the system. Generally the delay, mainly critical delay, happens due to the long multiplication process and the propagation delay is observed because of parallel adders in the addition stage. Multiplication is the fundamental operation of MAC unit. Power consumption, dissipation, area, speed and latency are the major issues in the multiplier unit. So, to avoid them, we go for fast multipliers in various applications of DSP, networking, etc.

Digital multipliers are the core components of all Digital signal processors. The speed of DSP is largely determined by the speed of its multipliers. Multiply Accumulate (MAC) operation is a commonly used operation in various Digital Signal Processing Applications. Use of a Digital Signal processor can significantly increase the performance of a MAC. Normally a multiply accumulate unit consists of a multiplier along with an accumulator which stores previous multiplication products. Since system performance widely depends on time needed to execute the instruction and multiplication being the most time consuming any improvement to multiplication will inherently improve the system performance. Multiplication can be implemented using several algorithms such as array, Booth, carry save, Modified Booth algorithm and Wallace tree in array multiplier multiplication of two numbers can be obtained with one micro operation. It is a fast method of multiplication since the only delay is time for the signals to propagate through the gates. But it requires larger number of gates and so it is less economical. In the carry save method, bits are processed one by one to supply a carry signal to an adder located at a one bit higher position. The limitation of this method is that its execution time depends upon the number of bits of the multiplier. In the Wallace tree method, the circuit layout is not easy although the speed of the operation is high. The method of Booth recording reduces the numbers of adders and hence the delay required to produce the partial sums. But the drawback is power consumption [1]. A new algorithm is developed that uses Vedic mathematics. The conventional mathematical algorithms can be simplified and even optimized by the use of Vedic mathematics. The implementation of MAC unit using Vedic multiplier the speed of MAC depends on the speed of the multiplier. The main goal of a DSP processor design to be enhance the speed of MACunit.

2. DESIGN & IMPLEMENTATION OF MAC USING VEDIC-MULTIPLIER

The multiply-accumulate unit computes the product of two numbers and adds that product to an accumulator. The 4- bit (Fig.3) MAC unit, consisting of a multiplier followed by an adder and an accumulator register which stores the result when clocked [4-5]. The output of the register is fed back to one input of the adder, so that on each clock the output of the multiplier is added to the register. Combinational multipliers require a large amount of logic, but can compute a product much more quickly than the method of shifting and adding typical of earlier computers. The MAC circuit must check for overflow,

Which might happen when the number of MAC operations is large. Overflow in a signed adder occurs when two operands with the same sign produce a result with a different sign.

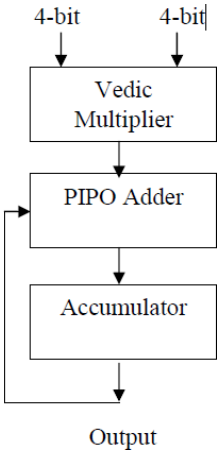


Fig.3: Block diagram of 4-bit MAC using PIPO Adder.

In this Paper the 8-bit MAC (Fig.4) is operated on the Urdhva-Triyakbhyam of Vedic Sutra, by using Vedic multiplier with parallel in parallel out adder. The multiplicand of 8-bits can give the product of 64-bits, by using the urdhav sutra the operation of multiplier and multiplicand can perform easily.

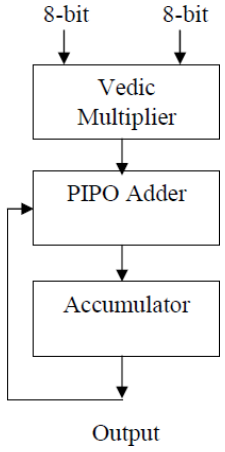


Fig.4: Block diagram of 8-bit MAC using PIPO adder.

Multiplication: Multiplication is a fundamental operation of MAC unit [1]. Multipliers have large area, long latency and consume considerable power. Fast multipliers are essential parts of digital signal processing systems. In order to improve the speed of the MAC unit, there are two major criteria's. The first is reducing the number of partial products in the multiplication block and the second is reducing burden of accumulator. As the multiplier consumes considerable delay among the basic operational blocks in digital system, the multiplier determines the critical path. In this section the MAC using the Vedic, Booth and Conventional multiplier.

Vedic multiplier: The main purpose of Vedic Mathematics is to be able to solve complex calculations by simple techniques (Fig.5). The formula being very short makes them practically simple in implementation. Urdhva Tiryagbhyam (Vertically and crosswise) sutra is general formula applicable to multiplication operation. Its algebraic principle is based on multiplication of polynomials. The Vedic multiplier using Urdhva Tiryagbhyam sutra of width NXN will generate the 2N-1 cross products of different widths which when combined forms (log2N+1) partial products. The partial products are obtained by vertical and crosswise operations using the Sutra. Hence the delay is equal to adder delay. Critical path would consist of adders adding the maximum number of bits in cross product. In all cases it will be the cross product in which all bits of multipliers are considered as shown in Fig.4.

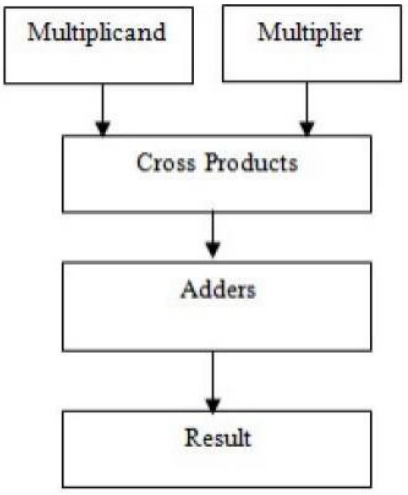
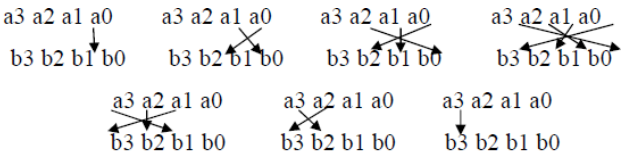


Fig.5: Architecture of Vedic Multiplier.

Accumulator: Accumulator is a type of register included in a CPU. It acts as a temporary storage location which holds an intermediate value in mathematical and logical calculations. Intermediate results of an operation are progressively written to the accumulator, overwriting the previous value. For example, in the operation 3+4+5 the accumulator would hold the value 3, then the value 7, then the value 12. The benefit of an accumulator is that it does not need to be explicitly referenced, which converses data in the operation statement.

3. MULTIPLICATION PROCESS ALGORITHMS

Multiplication Process for Urdhav: It has performs general formula applicable to all cases of multiplicationand also in the division of a large number by another large number. It means "Vertically and cross wise."



- **Ex: 4 bit mac**

a3 a2 a1 a0
b3 b2 b1 b0
---
a0b0
a1b0+b1a0
a2b0+a1b1+a0b2
a3b0+b3a0+b2a1+b1a2
a1b3+b2a2+a3b1
a2b3+a3b2
a3b3

Multiplication Process for Yavadunam: Squaring is an exclusive case of multiplication. Yavadunam sutra (Fig.6) has been used to square a number; it means that, "determine deficiency, lessen the deficiency from that number and write the square of the deficiency"

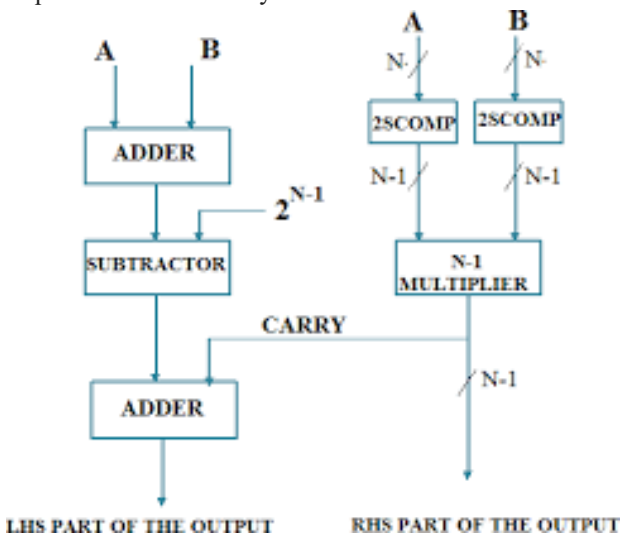


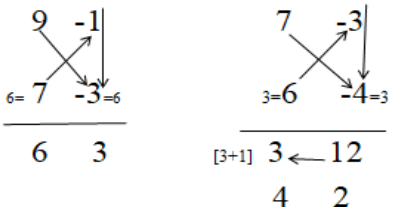
Fig.6: structure of yavadhunam process

Multiplication process for Nikhilam:

- Find the deviation of the given numbers from their bases.
- **Multiply** the deviation of the 2 given numbers.
- Add or subtract the deviations (based on whether the number is more or less than the base) from the base.

Ex:

All form 9 and last from 10



4. PROPOSEDTECHNIQUE

Parallel Input Parallel Output (PIPO) Adder:

The parallel in parallel out adder is the one of the shift register (Fig.7). This type of shift register also acts as a temporary storage device or as a time delay device similar to the SISO configuration. The data is presented in a parallel format to the parallel inputs pin PA to PD and then transferred together directly to their respective output pins QA to QD by the same clock pulse loads and unloads the register. This arrangement for parallel loading and unloading is shown below.

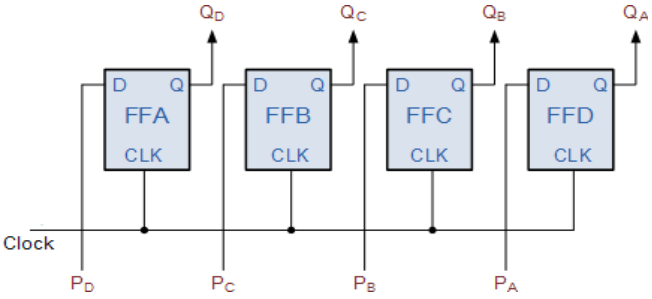


Fig7: PIPO shift register

5. RESULTS AND DISCUSSIONS

4-bit MAC design:

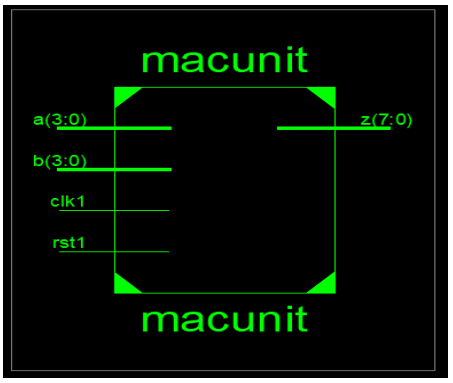


Fig.8: Schematic diagram for Yavadunam, Nikhilam & Urdhav

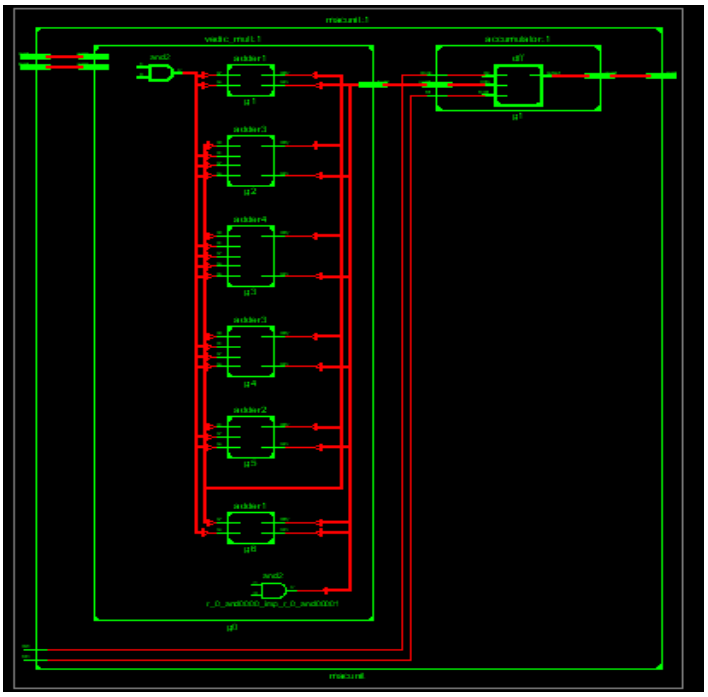


Fig.9: RTL Extraction Schematic diagram for yavadunam

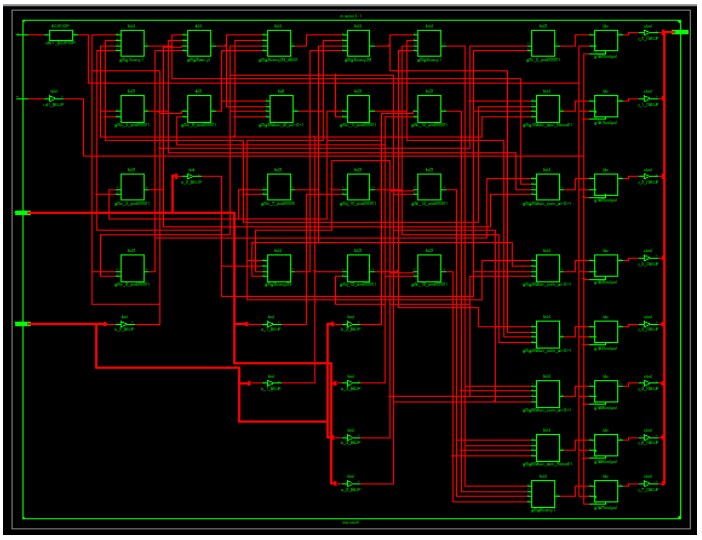


Fig.10: Technology Schematic diagram for yavadunam

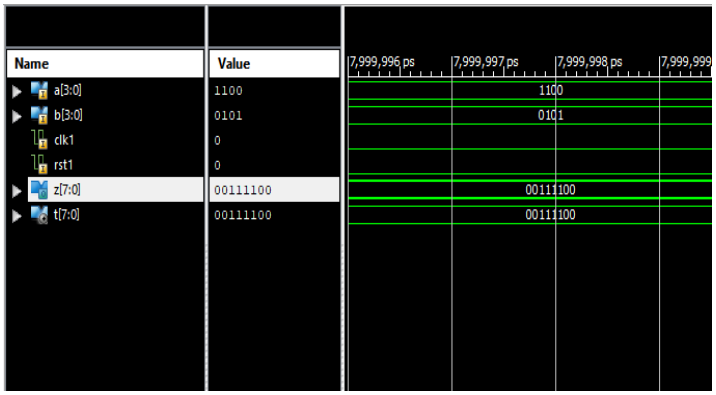


Fig.11: Output Waveform for yavadunam

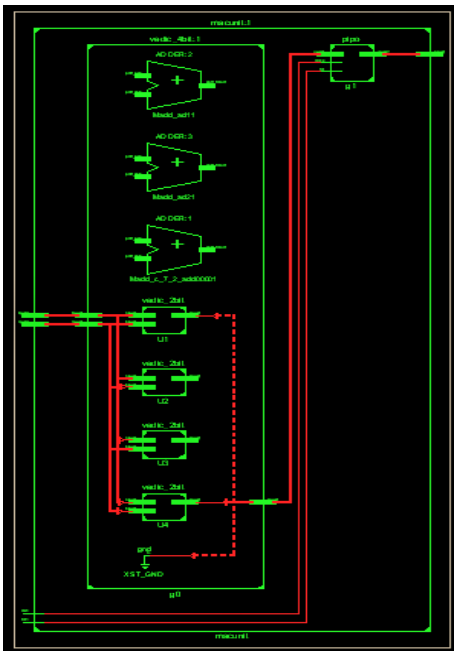


Fig.12: RTL Extraction Schematic diagram for Urdhav

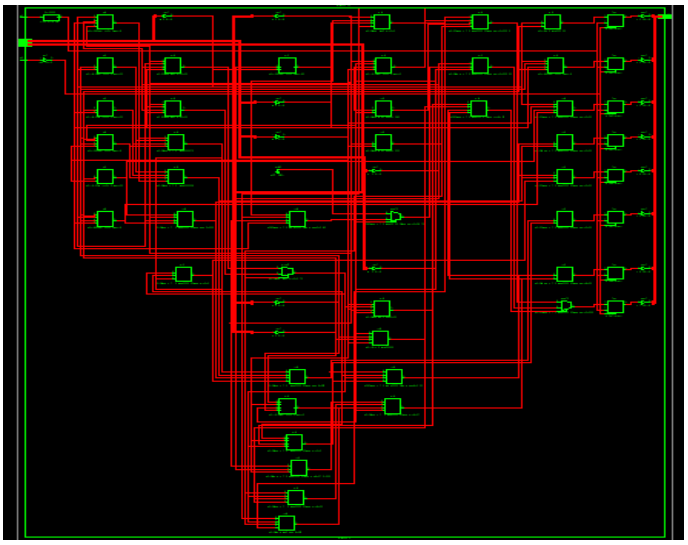


Fig.13: Technology Schematic diagram for Urdhav

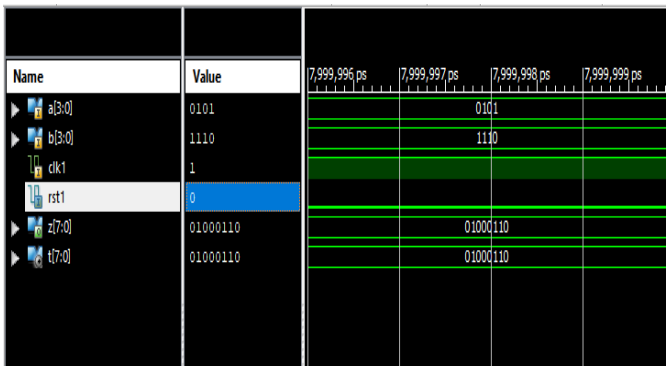


Fig.14: Output Waveform for Urdhav

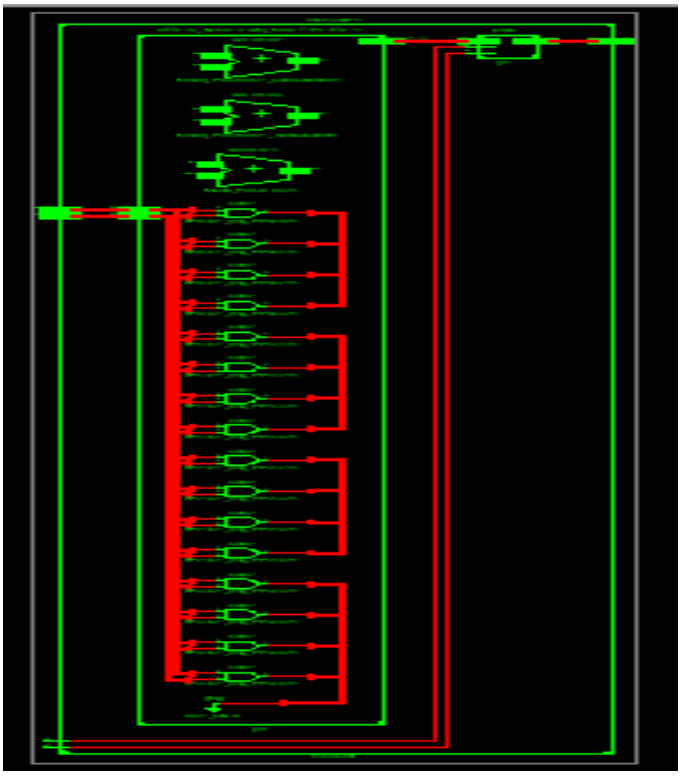


Fig.15: RTL Extraction schematic diagram for Nikhilam

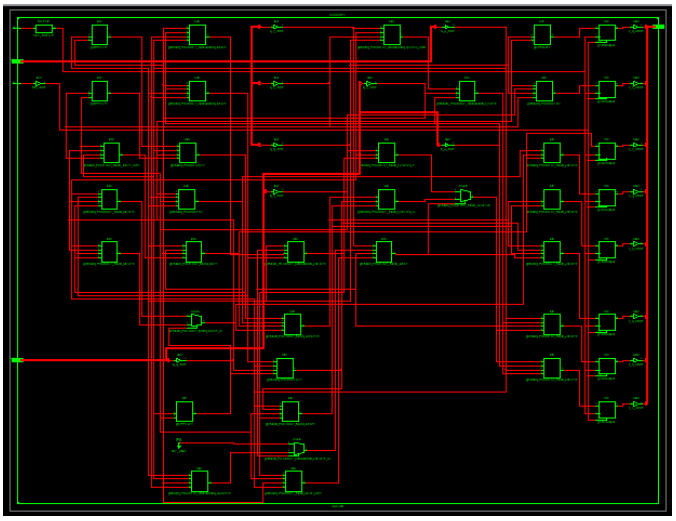


Fig.16: Technology schematic diagram for Nikhilam

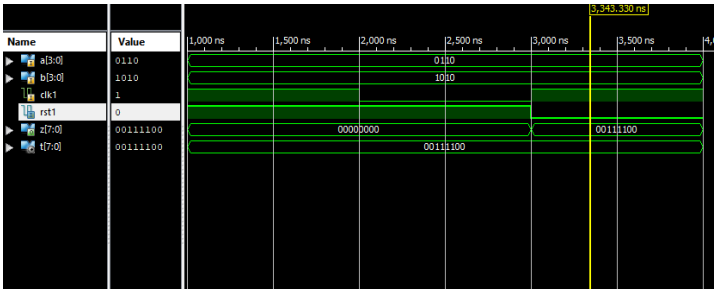


Fig.17: Output waveform for Nikhilam

8-bit MAC design by Urdhav Sutra:

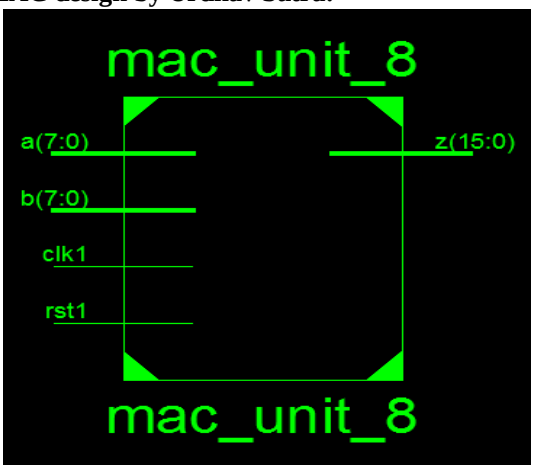


Fig.18: Schematic diagram

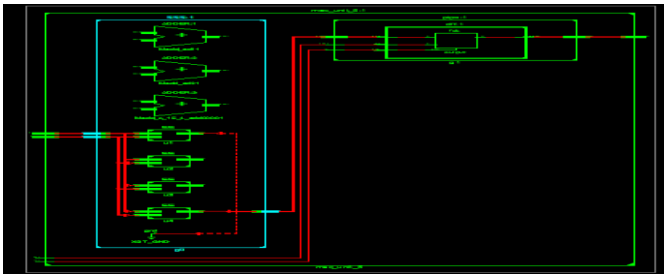


Fig.19: RTL Extraction Schematic diagram

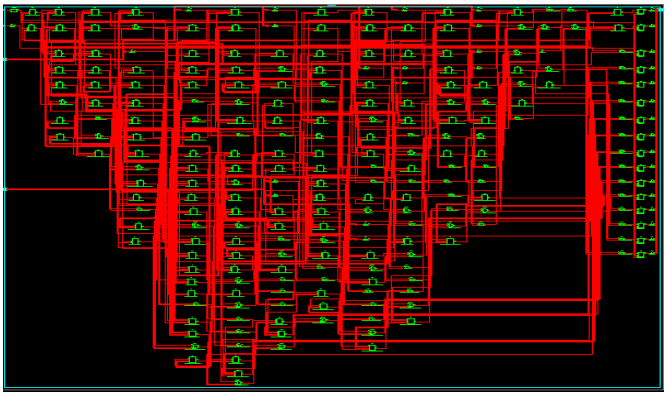


Fig.20: Technology schematic diagram

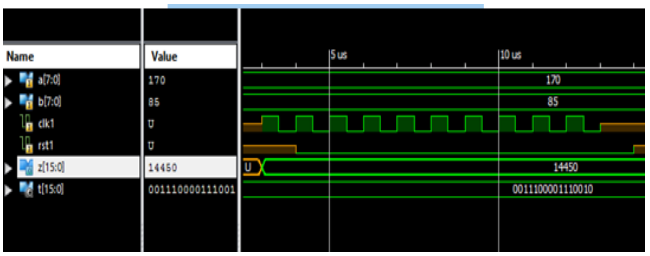


Fig21: Output Waveform

COMPARISON TABLE

Table.1: MAC by using Vedic square:

Logic utilization	Used
IOs	64
LUTs	727
ssssNo. Of Gates	747
No. Of accumulated instances	791

Table.2: Area comparison of Vedic multiplier

Vedic sutras	No. of Slices	No. of LUT's	No. Of bounded I/Os
MAC Urdhva	22	38	18
MAC Nikhilam	17	29	18
MAC Yavadunam	15	26	18

Table.3: Delay comparison of Vedic multiplier

Vedic sutras	Logic Delay	Routing Delay	Total Delay
MAC Urdhva	5.535ns	0.681ns	6.216ns
MAC Nikhilam	4.393ns	6.168ns	10.561ns
MAC Yavadunam	5.535ns	0.681ns	6.216ns

Table.4: 8-bit MAC by using Urdhav sutra:

Logic utilization	Used
Number of slices	68
Number of LUT's	123
Number of bonded IOBs	34
Number of GCKLs	1
Delay	16.489ns

6. CONCLUSION

From the comparison of area reports in Table1, 2 & 3, when the 16*16 bit Vedic square unit is simulated and synthesized in Vedic sutra of Urdhav. This Vedic square unit is only reduced area this is existed architecture. So, we have to introduce the Vedic multiplier this is the proposed architecture. In Vedic multiplier we can use 4-bit, this is simulated and synthesized in Vedic sutras of Urdhav, Yavadunam and Nikhilam. 8-bit is simulated and synthesized in Vedic sutras of Urdhav. The 4*4 and 8*8 bit proposed MAC module improved speed over optimized Vedic multiplier architecture. Hence the proposed MAC is very useful for high performance DSP processor. This reduction in number of gates also leads to an increase in speed and time delay will be reduced. Finally proposed MAC is executed in three Vedic sutras. So, table 2 & 3 is compared to the Yavadunam sutra is very efficient in are utilization of area and time delay.

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